Pulsed Hysteresis loop technique

This is an alternative method to obtain hysteresis loops for ferroelectric thin films that overcomes the drawbacks of the classical methods [1]. In this method, a pulsed signal, obtained by mixing a sinusoidal voltage of low frequency with a square voltage of variable period and width, is applied to the sample, yielding directly the loop. The electric field is reversed and it is applied to the sample for a short time so contributions to the loop coming from capacitance are suppressed and from leakage currents strongly reduced. The compensation of the contribution from leakage currents is performed by a graphical method that does not need to know a-priori the nature of this extra-current [1].

Experimental set-up

A sinusoidal pulsed electric field is obtained by blending a sinusoidal signal of frequencies in the range 0.01 Hz and 50 Hz., complete dielectric characterization as a function of frequency (10Hz-15 MHz) and temperature and (100 – 1400 K), and thermo-stimulated current measurements using dynamic and static methods to obtain the pyroelectric coefficient. All these characterization can be made at controlled atmospheres using the rigs available.

In the field of polar ceramics as thin films, new techniques of ferroelectric characterization like the pulsed hysteresis loop has been developed. This technique is able to measure in an easy way the first hysteresis loop, fundamental in the studies of self-polarization in ferroelectric thin films. Also the characterization of thin film NVFeRAM capacitors endurance reproducing the writing and reading conditions of a computer has been also developed using a FPGA tool.

Endurance test of NVFeRAM

To evaluate a single ferroelectric memory cell in real conditions, it has been developed a characterisation system. The memory cell is a single ferroelectric capacitor and a pass transistor that controls the access to its logic state by the word line. Read and write operations are generated by a field programmed gate array, FPGA. To read the memory state, the bit line is connected to a sense amplifier that is a reference capacitor. A control process unit, CPU, requests a write and read operation to the FPGA. Time between write and read operation, td and write/read cycle operations depend on CPU tasks. To read a stored “1” a negative voltage must be used and a switching current will charge the reference capacitor to a level higher than in the case of a “0”, since in the last case there is not switching. At the present, a voltage > 2.5 V in the reference capacitor means a logic “1” meanwhile up to 2.0 V corresponds to a “0”. The characterisation system is monitored by a personal computer, PC. Data collection process consists on several sets of consecutive tests of fatigue and retention. The signal parameters can be selected using the software developed in testpoint, figure 4, in order to approach how a computer deal with data.

Bibliography


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