Thermal Scanning Probe Lithography: nano-patterning and nano-devices with high-resolution, within less processing steps, on novel materials.

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An Atomic Force Microscope (AFM) can imaging molecules with atomic resolution. It also can fold and unfold a protein at high speed to study molecular dynamics. It can give information about the mechanical, compositional, electrical, magnetic properties of biological samples, polymers, metals, semiconductors, which are very small in size with high resolution.

All the above mentioned capabilities are possible when a researcher uses an AFM as a characterization tool with minimal sample modification. On the opposite direction, if the intention is the direct modification of a material in a localized area at the nanoscale, then, the researcher will use an AFM in the technique called Scanning Probe Lithography (SPL). In SPL, the AFM tip is approached until contact to or over a few nanometers above the surface of a material. Depending on the type of this material, a thermal, electrical, mechanical or diffusive stimulus will be applied to fabricate patterns. High resolution is achievable since only the area close to a sharp tip will be modified. SPL is a maskless technique performed under ambient conditions applicable to any kind of materials. Unlike optical lithography, it does not have diffraction limit. Unlike electron beam lithography, it does not have proximity effect or possible charging disturbance. Two factors that favors SPL in terms of resolution and overlay accuracy. Since it is a serial technique, there exists a limitation in the throughput that is being addressed by high-speed, parallel approach and tip-endurance improvement.

Some of the last results on thermal Scanning Probe Lithography (t-SPL) are being presented in the seminar: It is able to pattern arrays of 14 nm half-pitch lines that are transferable to a targeted substrate by reactive ion etching processing through a transfer stack in a reproducible manner and without losing the resolution defined by the t-SPL fabricated pattern. The same process is used to a) make single electron transistors on an ultrathin silicon on insulator with sub-25 nm wide constrictions by etching the silicon and b) to make source-to-drain contacts with 50 nm distance on an InAs nanowire by lift-off processing. Finally, the same process is applicable to pattern sub-20 nm wide nanoribbons on MoS_2 monolayers-based field-effect transistors.